FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20834-2E

FLASH MEMORY

CMOS

4M (512K × 8/256K × 16) BIT

MBM29LV400T-12-X/MBM29LV400B-12-X

■ FEATURES

- **Single 3.0 V read, program, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  48-pin TSOP (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  44-pin SOP (Package suffix: PF)
  46-pin SON (Package suffix: PN)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  120 ns maximum access time
- **Sector erase architecture**
  One 16K byte, two 8K bytes, one 32K byte, and seven 64K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detector of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations

(Continued)

MBM29LV400T-12-X/MBM29LV400B-12-X

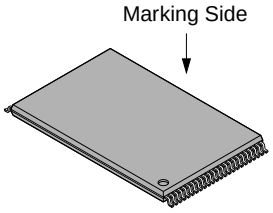
(Continued)

- **Temporary sector unprotection**
  Hardware method enables temporarily any combination of sectors from program or erase operations.
- **Extended operating temperature range: –40°C to +85°C**

Please refer to MBM29LV400T/MBM29LV400B data sheet in detailed specifications.

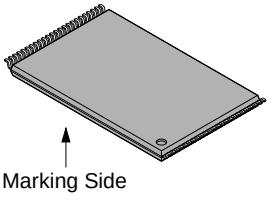
■ PACKAGE

48-pin Plastic TSOP (I)



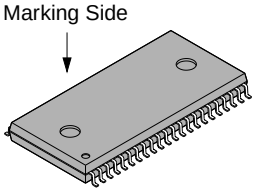
(FPT-48P-M19)

48-pin Plastic TSOP (I)



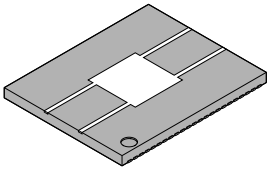
(FPT-48P-M20)

44-pin Plastic SOP



(FPT-44P-M16)

46-pin Plastic SON



(LCC-46P-M02)

■ DESCRIPTION

The MBM29LV400T-X/B-X are a 4M-bit, 3.0 V-only Flash memory organized as 512K bytes of 8 bits each or 256K words of 16 bits each. The MBM29LV400T-X/B-X are offered in 48-pin TSOP, 44-pin SOP and 46-pin SON packages. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV400T-X/B-X offer access time 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The MBM29LV400T-X/B-X are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV400T-X/B-X are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

Any individual sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV400T-X/B-X are erased when shipped from the factory.

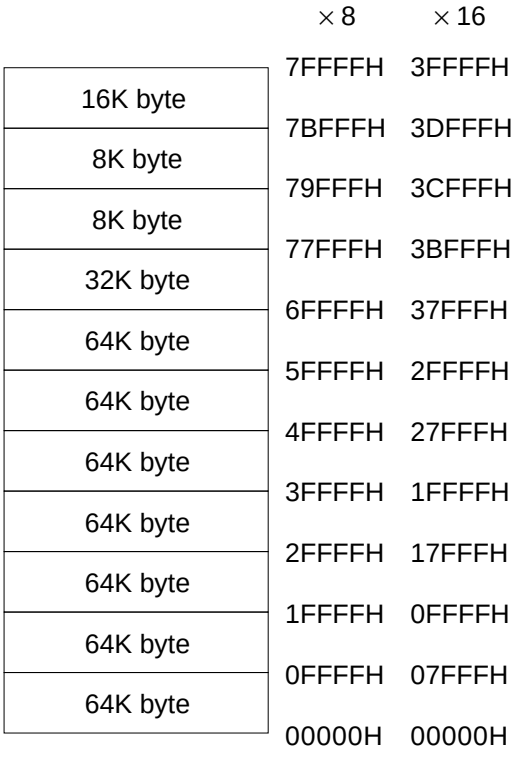
The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The MBM29LV400T-X/B-X memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

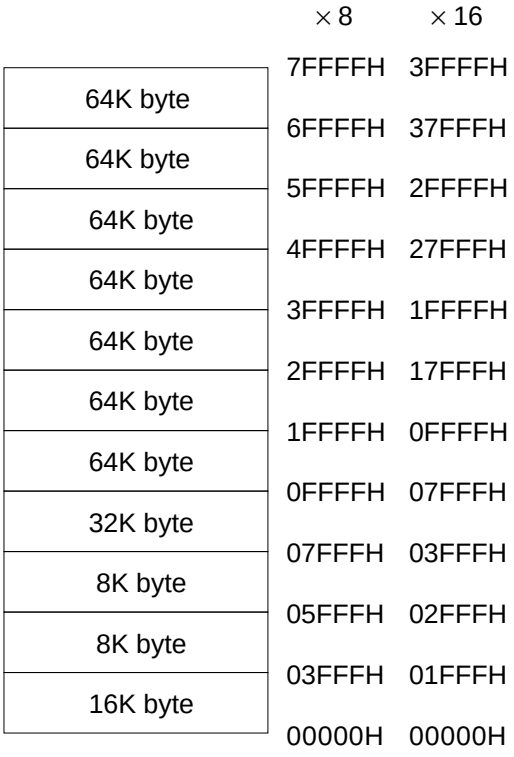
MBM29LV400T-12-X/MBM29LV400B-12-X

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16K byte, two 8K bytes, one 32K byte and seven 64K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.
- Individual or multiple-sector protection is user definable.



MBM29LV400T-X Sector Architecture



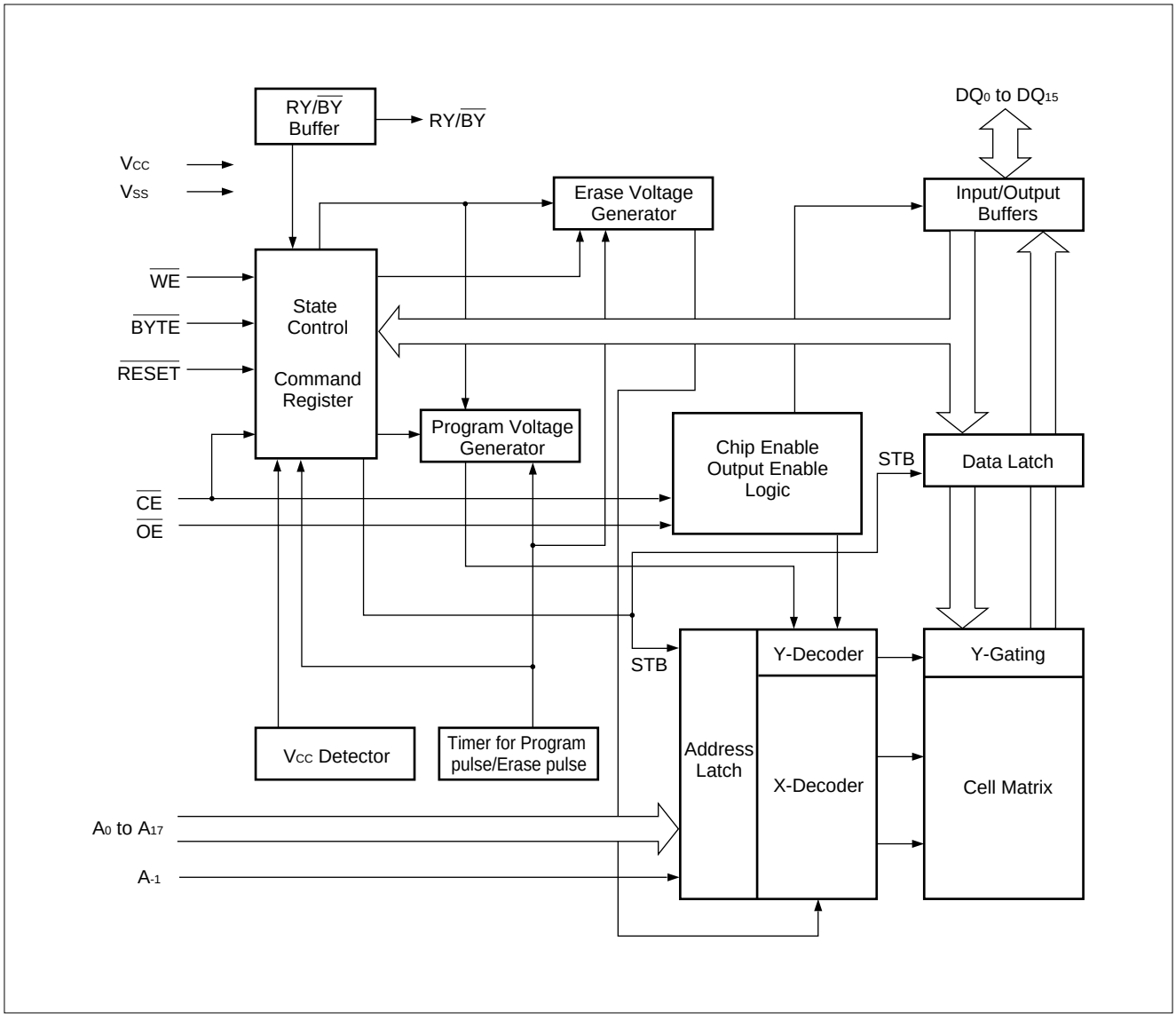
MBM29LV400B-X Sector Architecture

■ PRODUCT LINEUP

Part No.	MBM29LV400T-X/MBM29LV400B-X
Ordering Part No.	-12
Max. Address Access Time (ns)	120
Max. $\overline{CE}$ Access Time (ns)	120
Max. $\overline{OE}$ Access Time (ns)	50

MBM29LV400T-12-X/MBM29LV400B-12-X

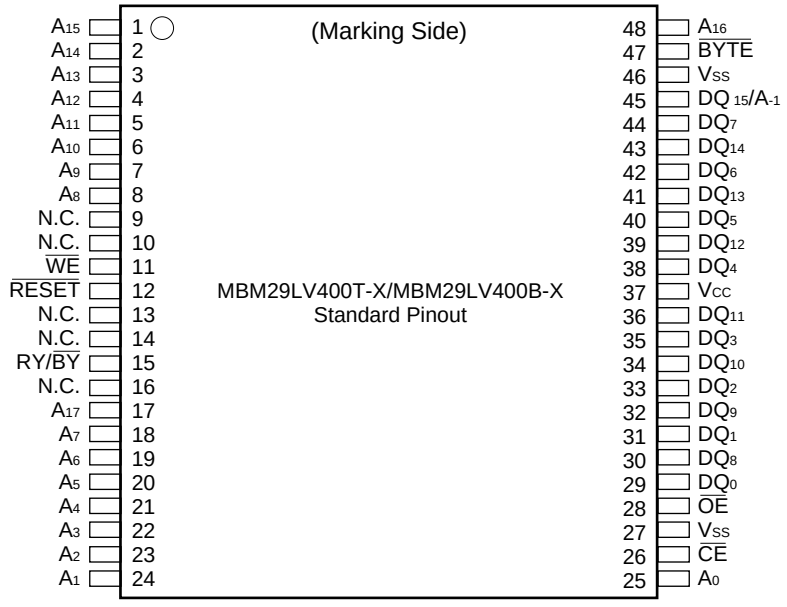
■ BLOCK DIAGRAM



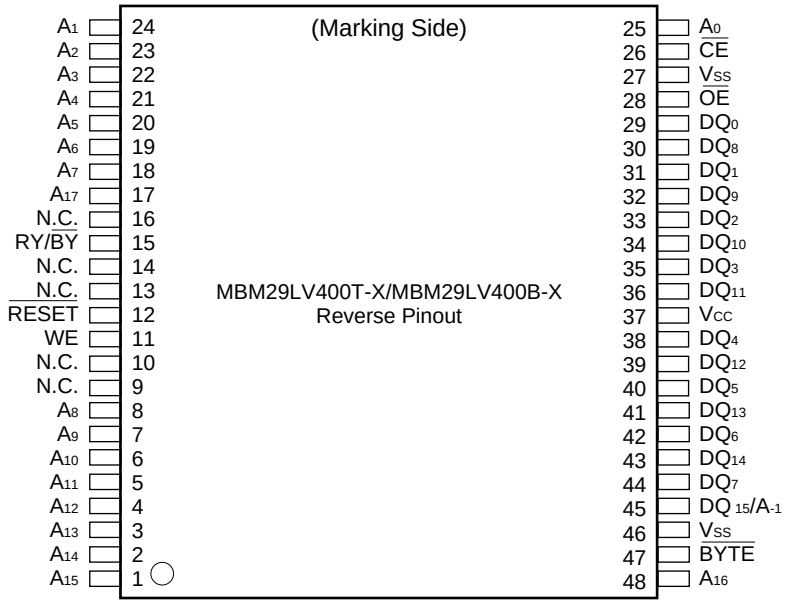
MBM29LV400T-12-X/MBM29LV400B-12-X

■ CONNECTION DIAGRAMS

TSOP

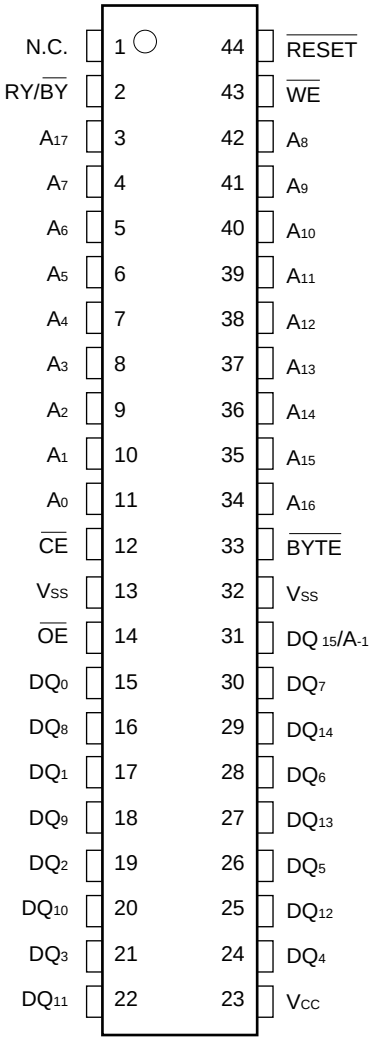


FPT-48P-M19



FPT-48P-M20

SOP
(Top View)



FPT-44P-M16

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MBM29LV400T-12-X/MBM29LV400B-12-X

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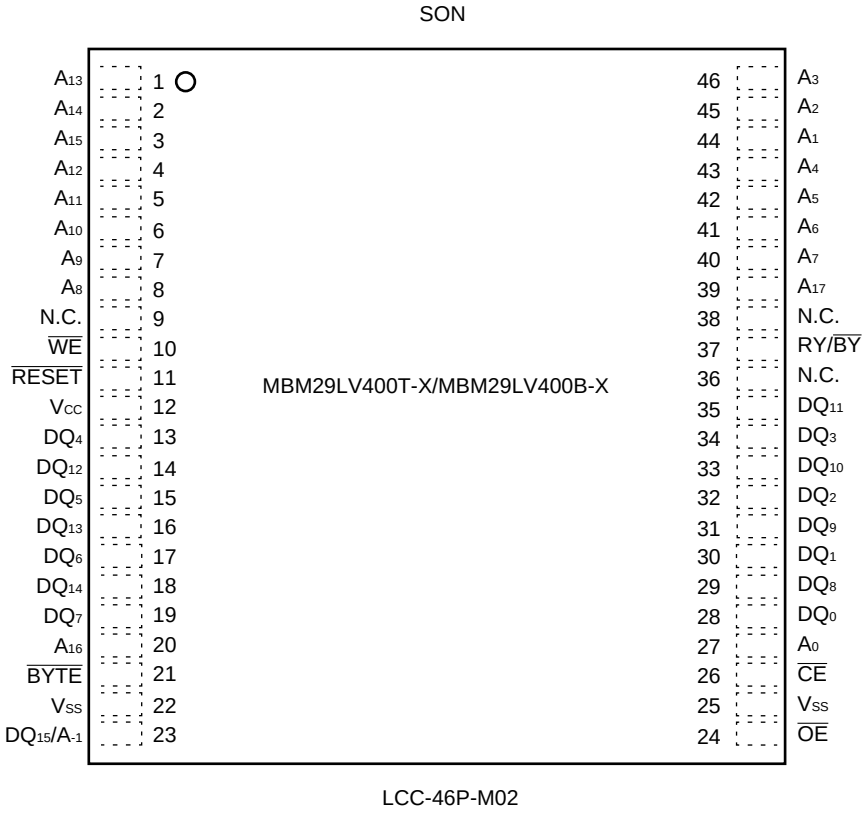


MBM29LV400T-12-X/MBM29LV400B-12-X

■ LOGIC SYMBOL

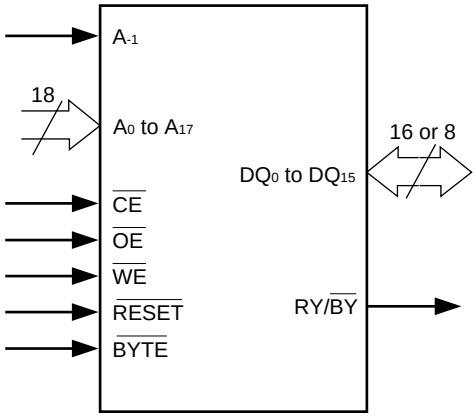


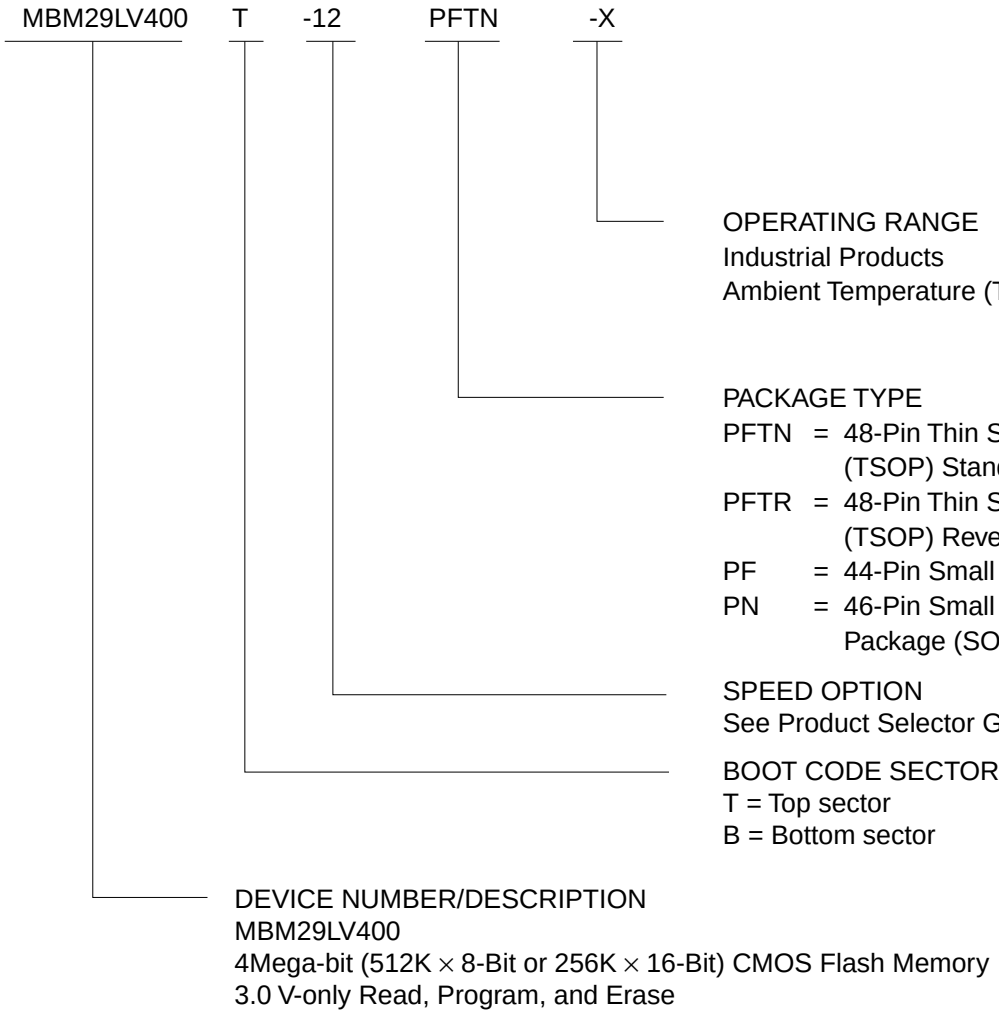
Table 1 MBM29LV400T-X/400B-X Pin Configuration

Pin	Function
A_{-1}, A_0 to A_{17}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Outputs
$\overline{RESET}$	Hardware Reset Pin/ Sector Protection Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply (3.0 V $^{+0.6\ V}_{-0.3\ V}$)

■ ORDERING INFORMATION

Industrial Products

Fujitsu Industrial products are available in several packages. The order number is formed by a combination of:



■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +125°C
Ambient Temperature with Power Applied..... –40°C to +85°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, and $\overline{RESET}$ (Note 1)..... –0.5 V to V_{CC}+0.5 V
V_{CC} (Note 1) ..... –0.5 V to +5.5 V
A_9, $\overline{OE}$, and $\overline{RESET}$ (Note 2) ..... –0.5 V to +13.0 V

Notes: 1. Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A_9, $\overline{OE}$, and $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins are +13.0 V which may overshoot to 14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Industrial Devices
Ambient Temperature (T_A) ..... –40°C to +85°C

V_{CC} Supply Voltages ..... +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ MAXIMUM OVERSHOOT

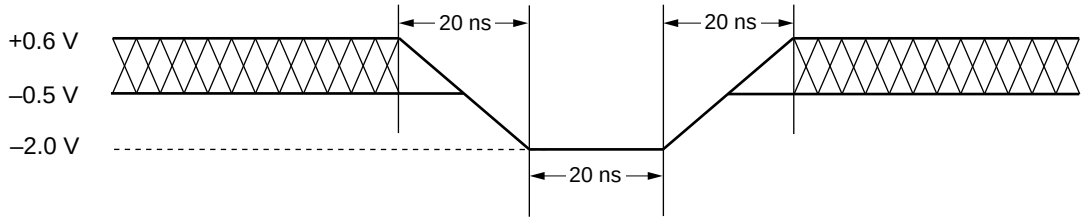


Figure 1 Maximum Negative Overshoot Waveform

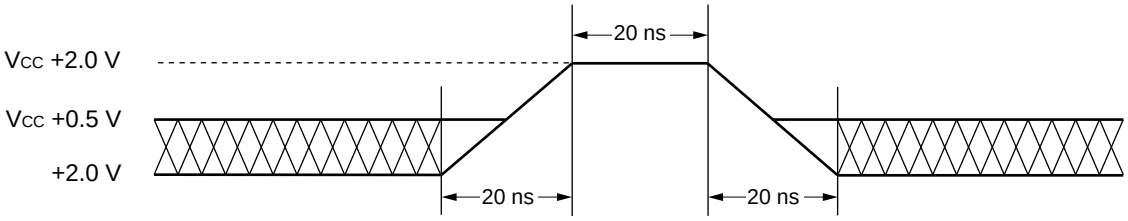
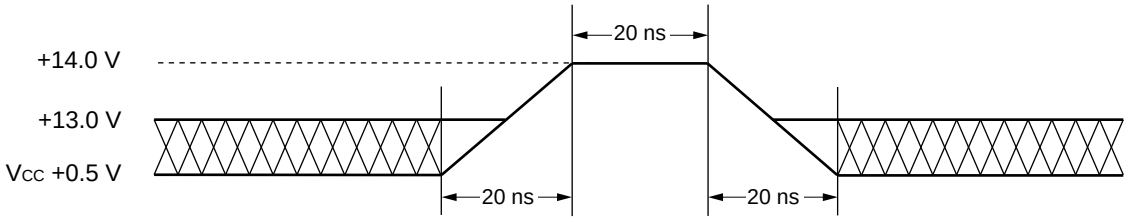


Figure 2 Maximum Positive Overshoot Waveform



*: This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max., A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	80	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte	—	30	mA
			Word		35	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	35	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V		—	50	µA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V		—	50	µA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		2.0	V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$)	—		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min.		2.4	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.		V_{CC} – 0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		2.3	2.5	V

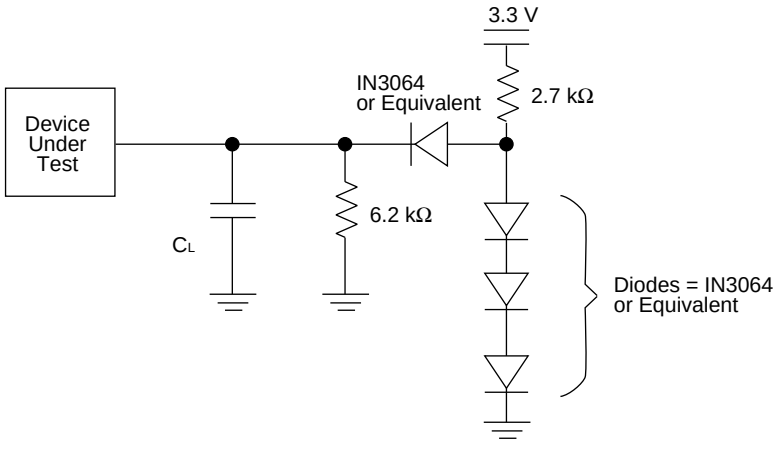
Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz).
The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

■ AC CHARACTERISTICS

- **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup		-12 (Note)	Unit
JEDEC	Standard					
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max.	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	ns

Notes: Test Conditions: Output Load: 1 TTL gate and 100 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V



Notes: C_L = 100 pF including jig capacitance

Figure 4 Test Conditions

- **Write/Erase/Program Operations**
  Alternate $\overline{WE}$ Controlled Writes

Parameter Symbols		Description			-12	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	ns
			Toggle and $\overline{Data}$ Polling	Min.	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	sec
—	t_{VCS}	V_{CC} Setup Time		Min.	50	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	µs
—	t_{RB}	Recover Time From RY/$\overline{BY}$		Min.	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		Min.	500	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		Max.	40	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min.	90	ns

Notes: 1. This does not include the preprogramming time.
2. These timings are for Sector Protection operation.

- **Write/Erase/Program Operations**
  Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			-12	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min.	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min.	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min.	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	ns
			Toggle and $\overline{Data}$ Polling	Min.	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min.	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min.	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)		Typ.	1	sec
—	t_{VCS}	V_{CC} Setup Time		Min.	50	µs
—	t_{RB}	Recover Time From RY/$\overline{BY}$		Min.	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		Min.	500	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		Max.	40	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min.	90	ns

Note: This does not include the preprogramming time.

■ SWITCHING WAVEFORMS

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	H or L Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

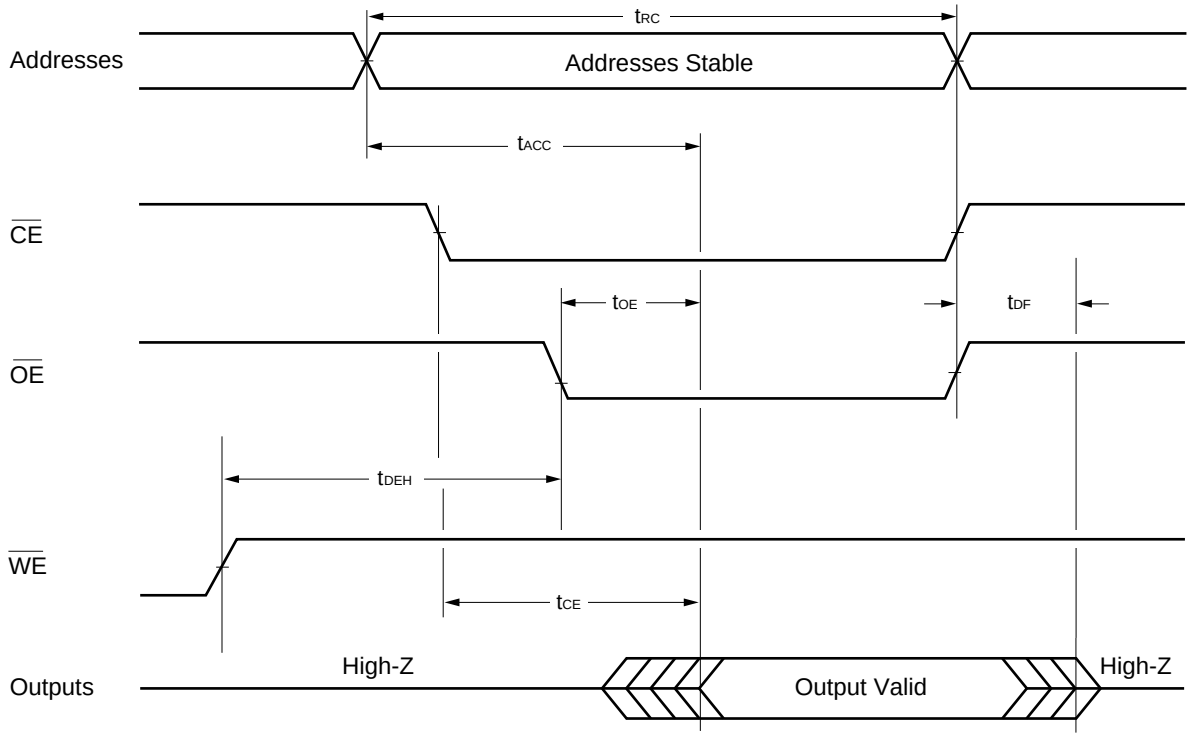


Figure 5.1 AC Waveforms for Read Operations

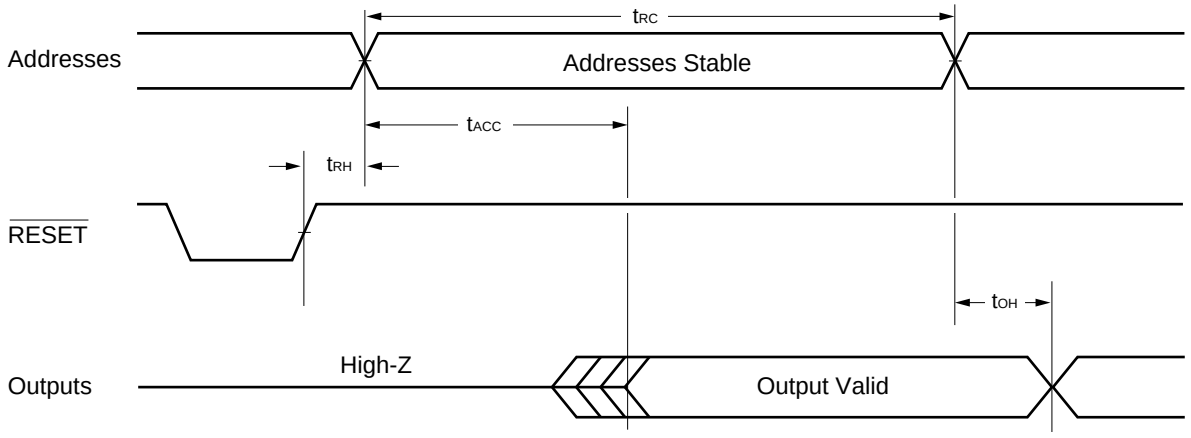
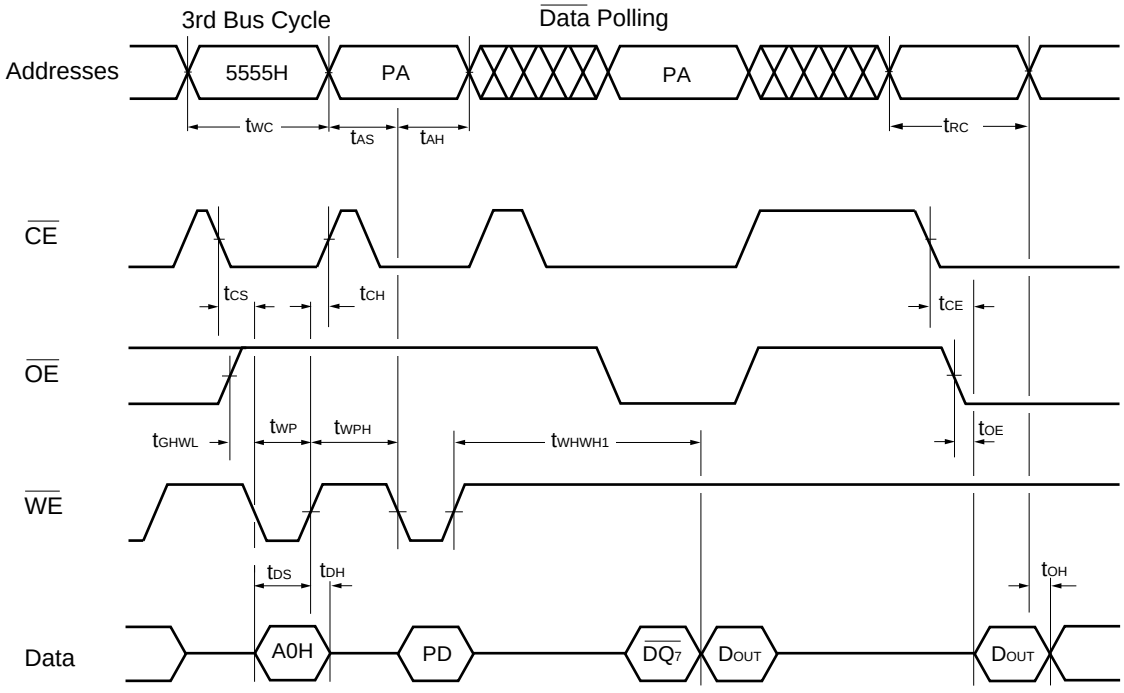
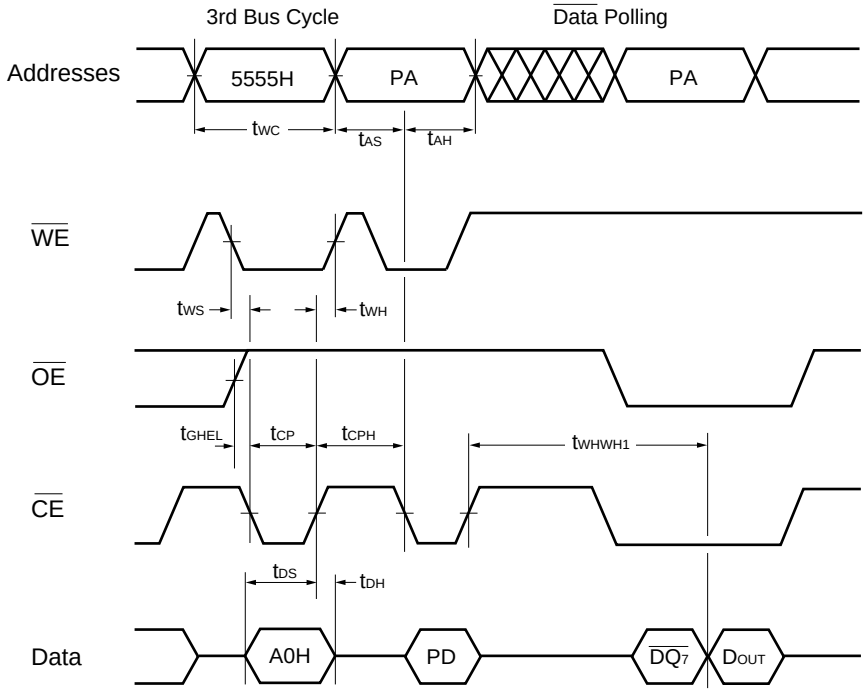


Figure 5.2 AC Waveforms for Hardware Reset/Read Operations



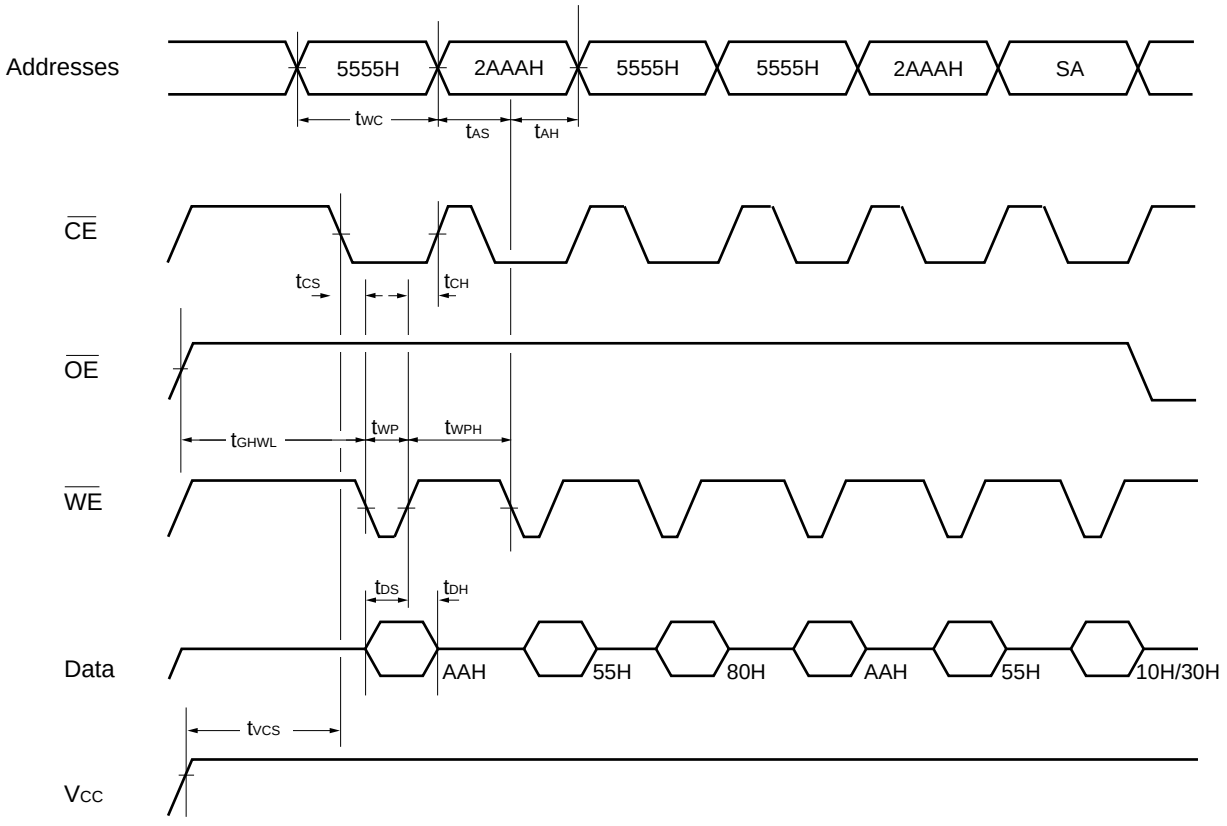
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the ×16 mode. The addreses differ from ×8 mode.

Figure 6 Alternate $\overline{WE}$ Controlled Program Operation Timings



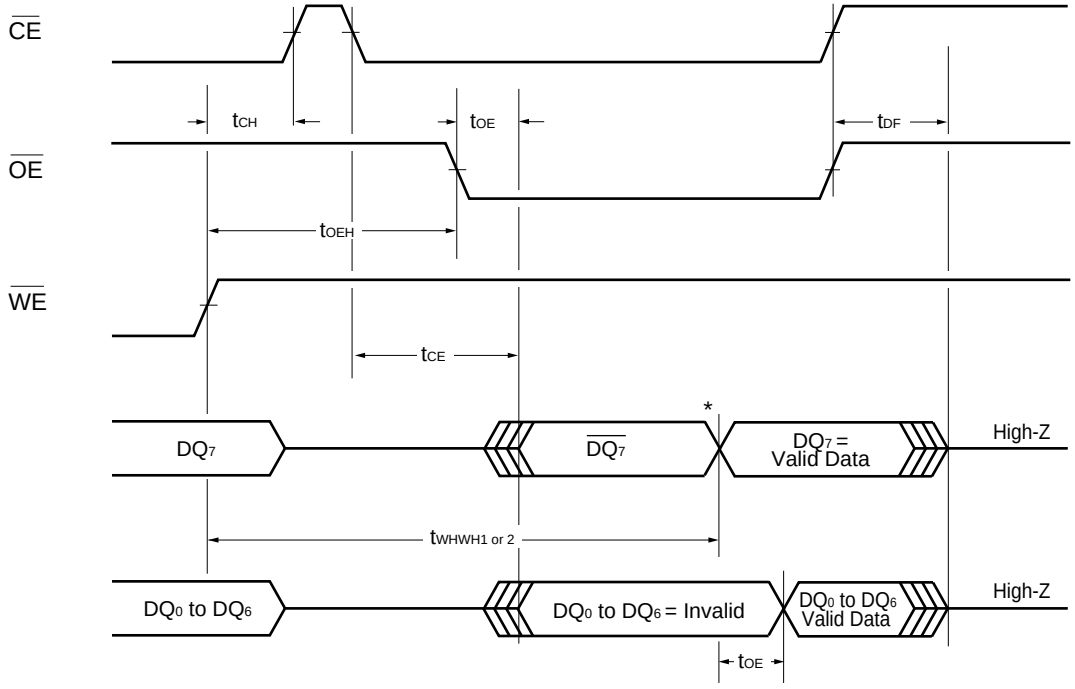
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These wavefororms are for the ×16 mode. The addresses differ from ×8 mode.

Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timings



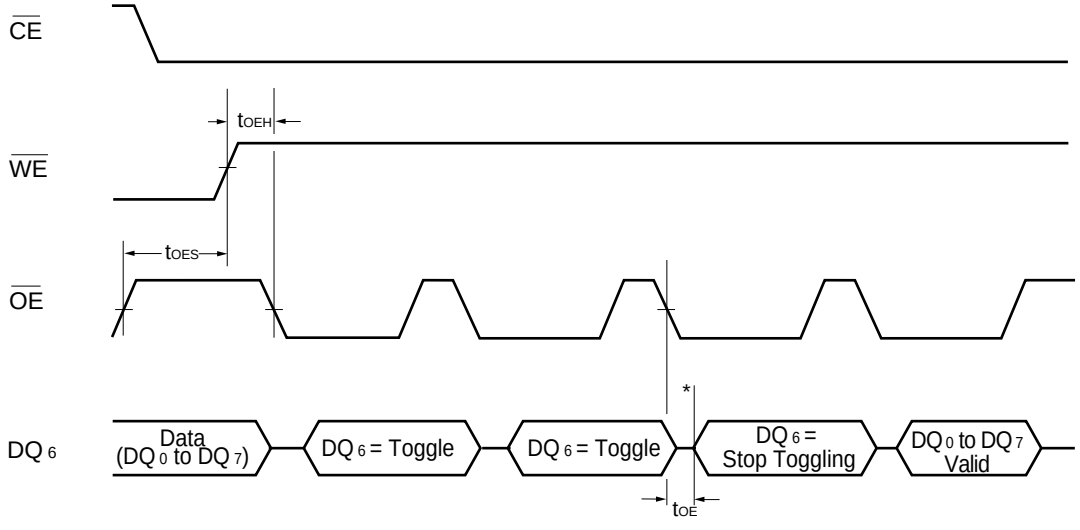
Notes: 1. SA is the sector address for Sector Erase. Addresses = 5555H (Word), AAAAH (Byte) for Chip Erase.
2. These waveforms are for the ×16 mode. The addresses differ from ×8 mode.

Figure 8 AC Waveforms Chip/Sector Erase Operations



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Figure 9 AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations



* : DQ_6 stops toggling (The device has completed the Embedded operation.)

Figure 10 AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

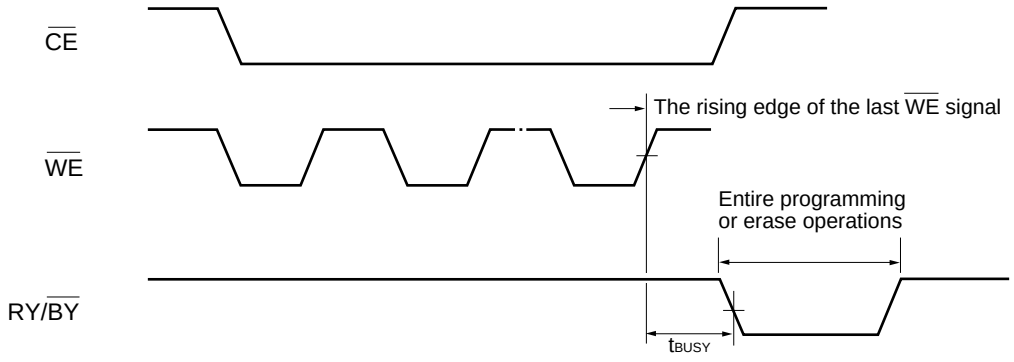


Figure 11 RY/BY Timing Diagram during Program/Erase Operations

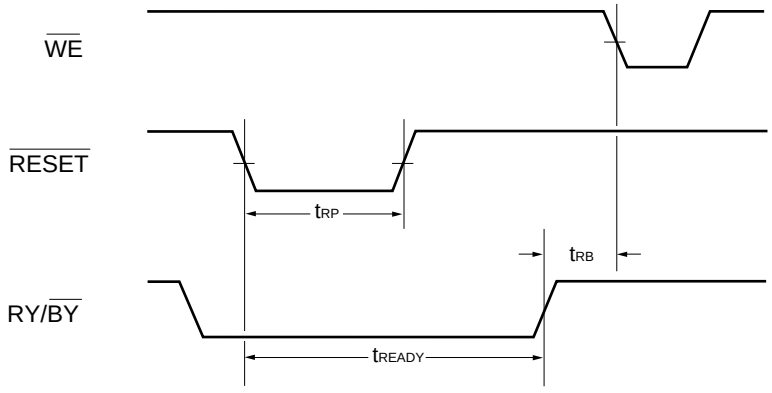


Figure 12 RESET, RY/BY Timing Diagram

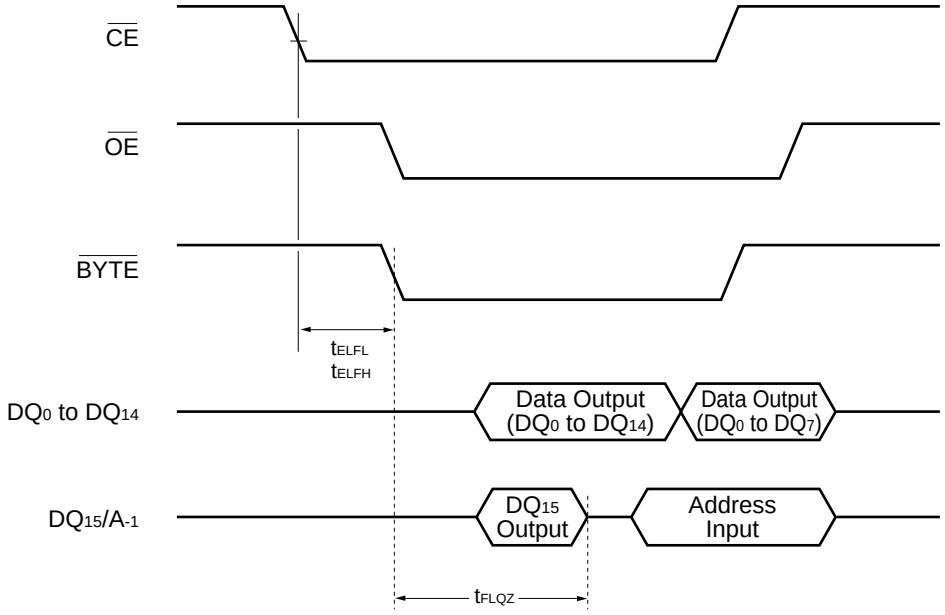


Figure 13 $\overline{\text{BYTE}}$ Timing Diagram for Read Operations

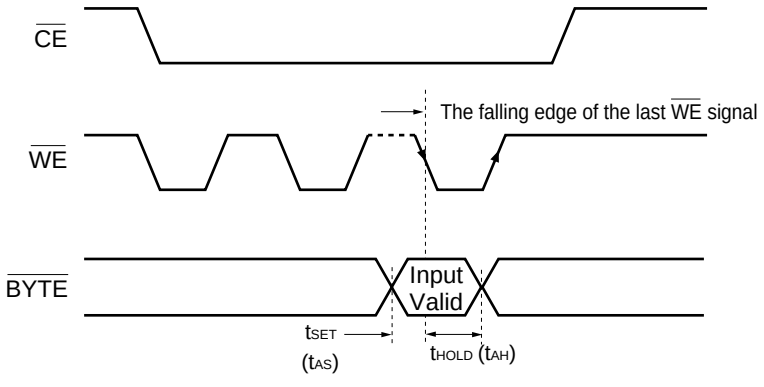
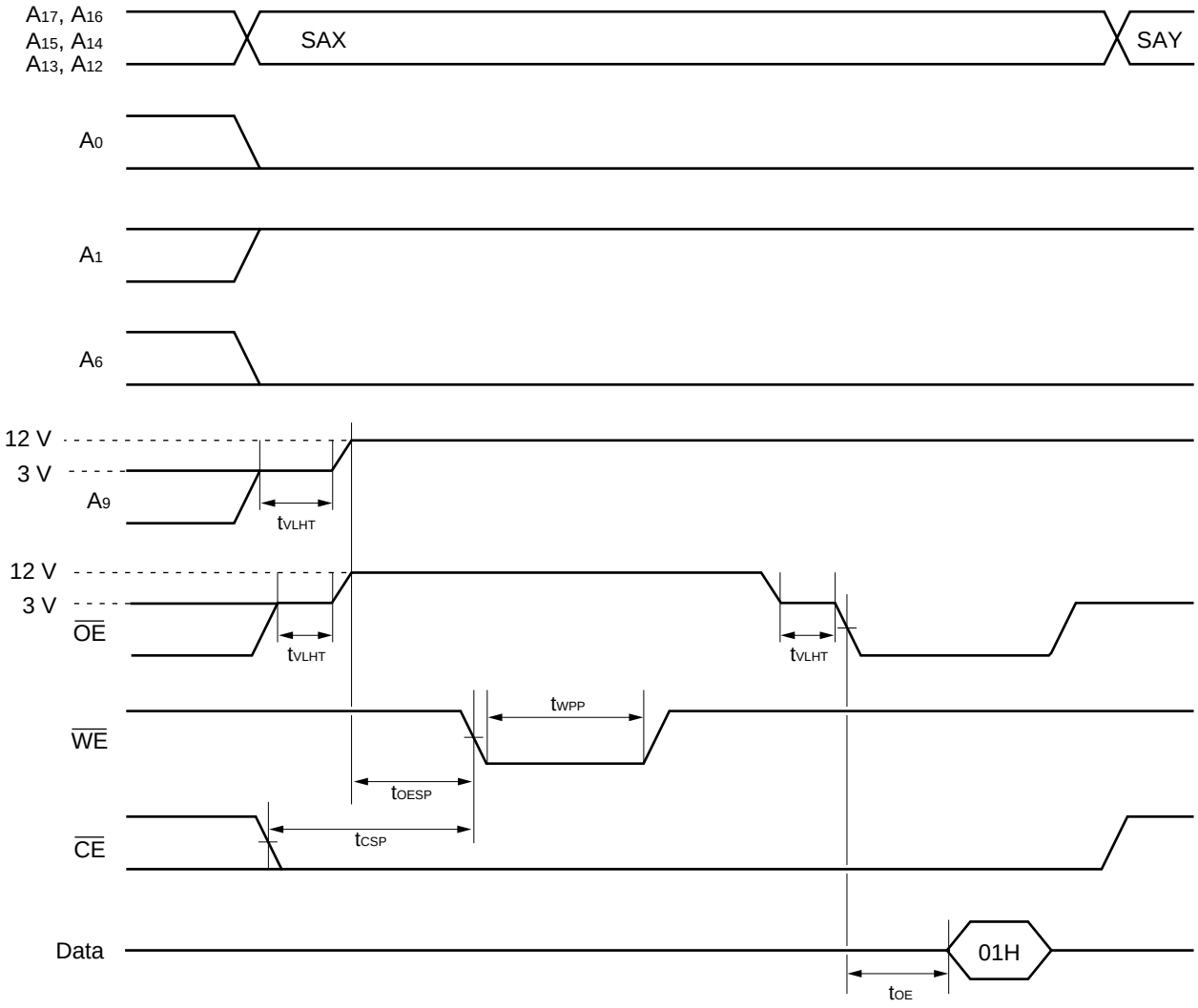


Figure 14 $\overline{\text{BYTE}}$ Timing Diagram for Write Operations



SAX : Sector Address for initial sector
SAY : Sector Address for next sector

Note: A_{-1} is V_{IL} on byte mode.

Figure 15 AC Waveforms for Sector Protection

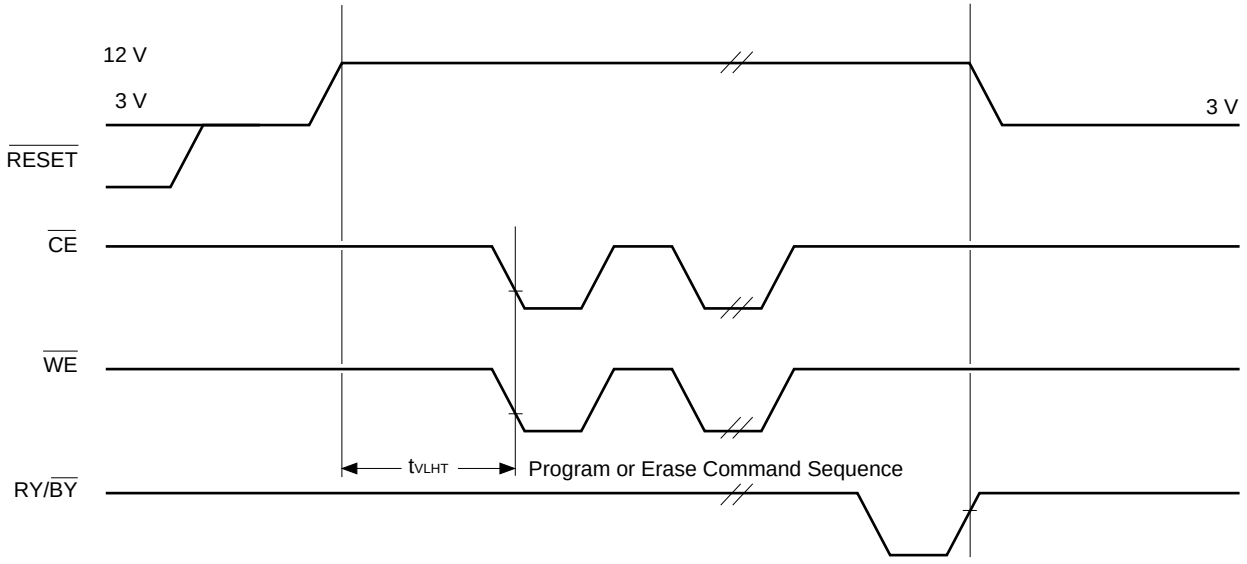
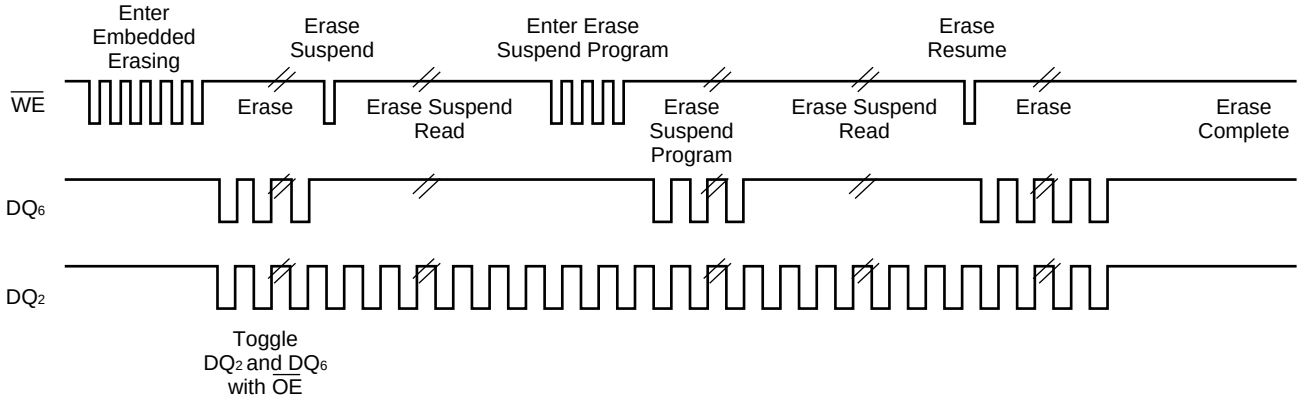


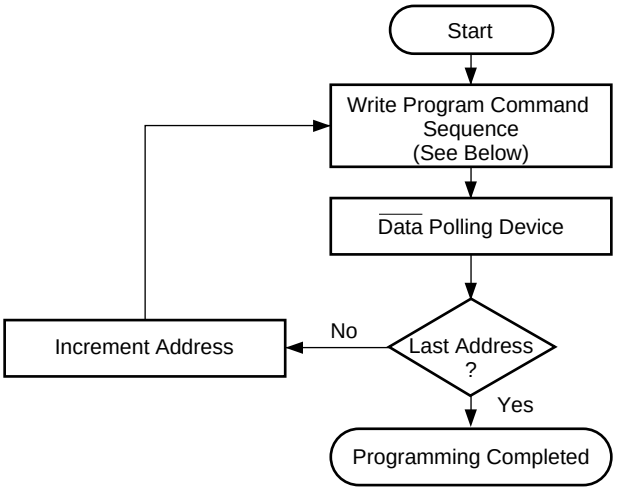
Figure 16 Temporary Sector Unprotection



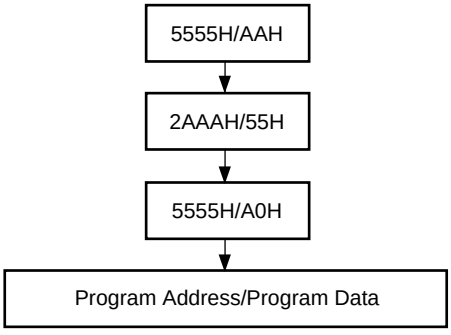
Note: DQ_2 is read from the erase-suspended sector.

Figure 17 DQ_2 vs. DQ_6

EMBEDDED ALGORITHMS



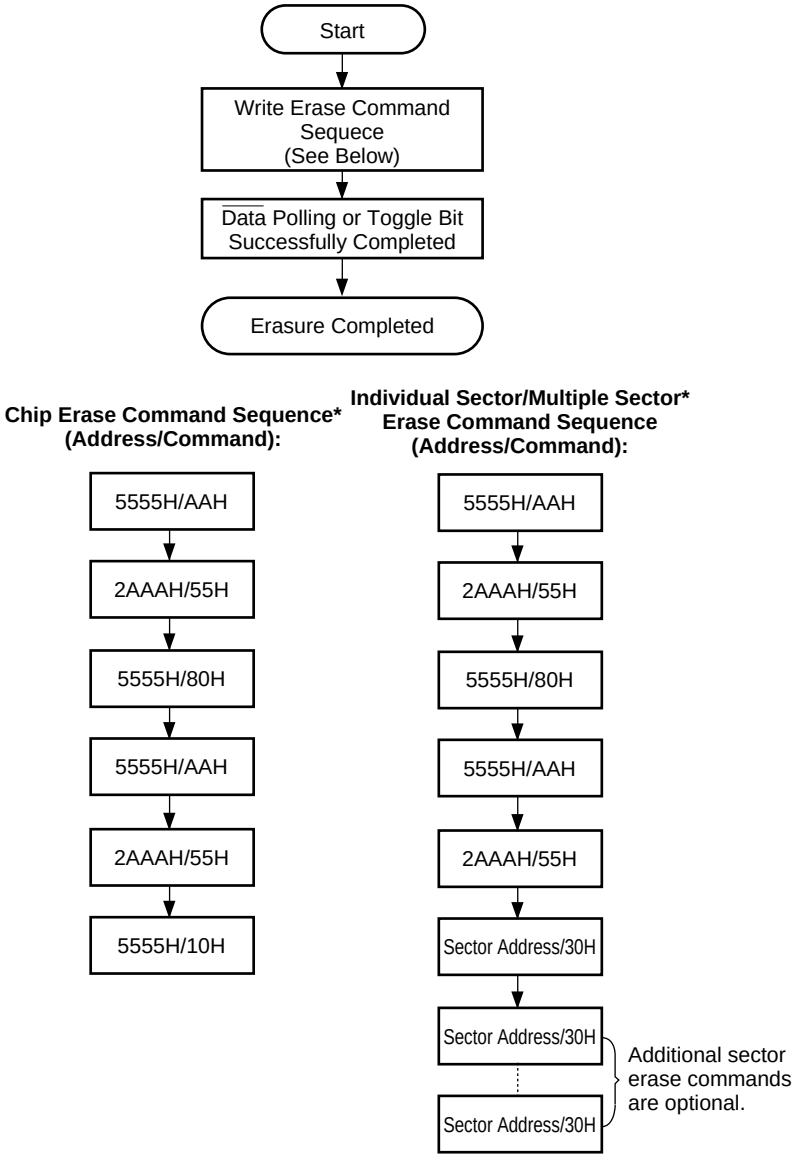
Program Command Sequence* (Address/Command):



* : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

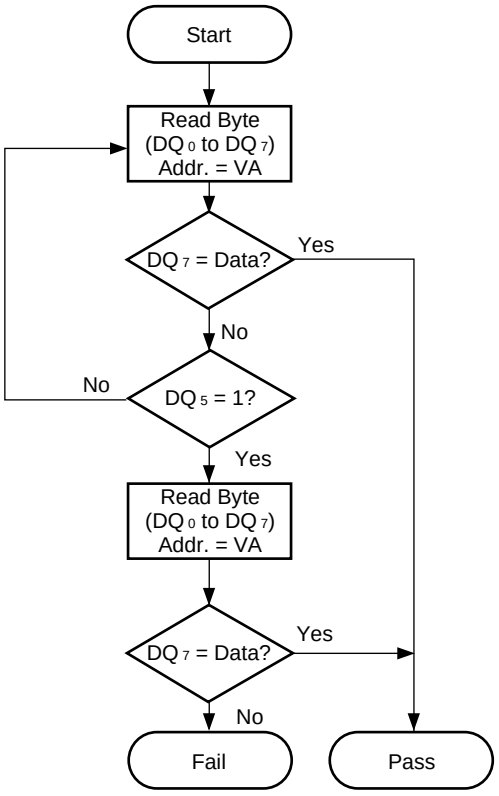
Figure 18 Embedded Programming™ Algorithm

EMBEDDED ALGORITHMS



* : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

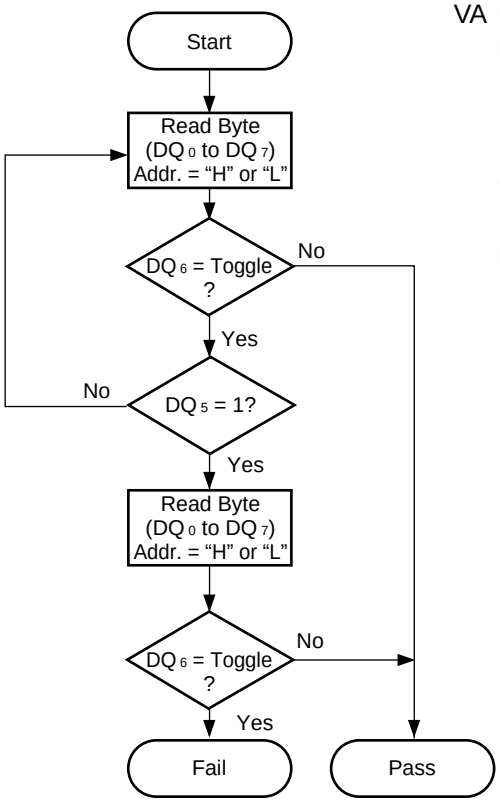
Figure 19 Embedded Erase™ Algorithm



VA = Byte address for programming.
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation.
= XXXXH during sector erase or multiple sector erases operation.
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

Note: DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

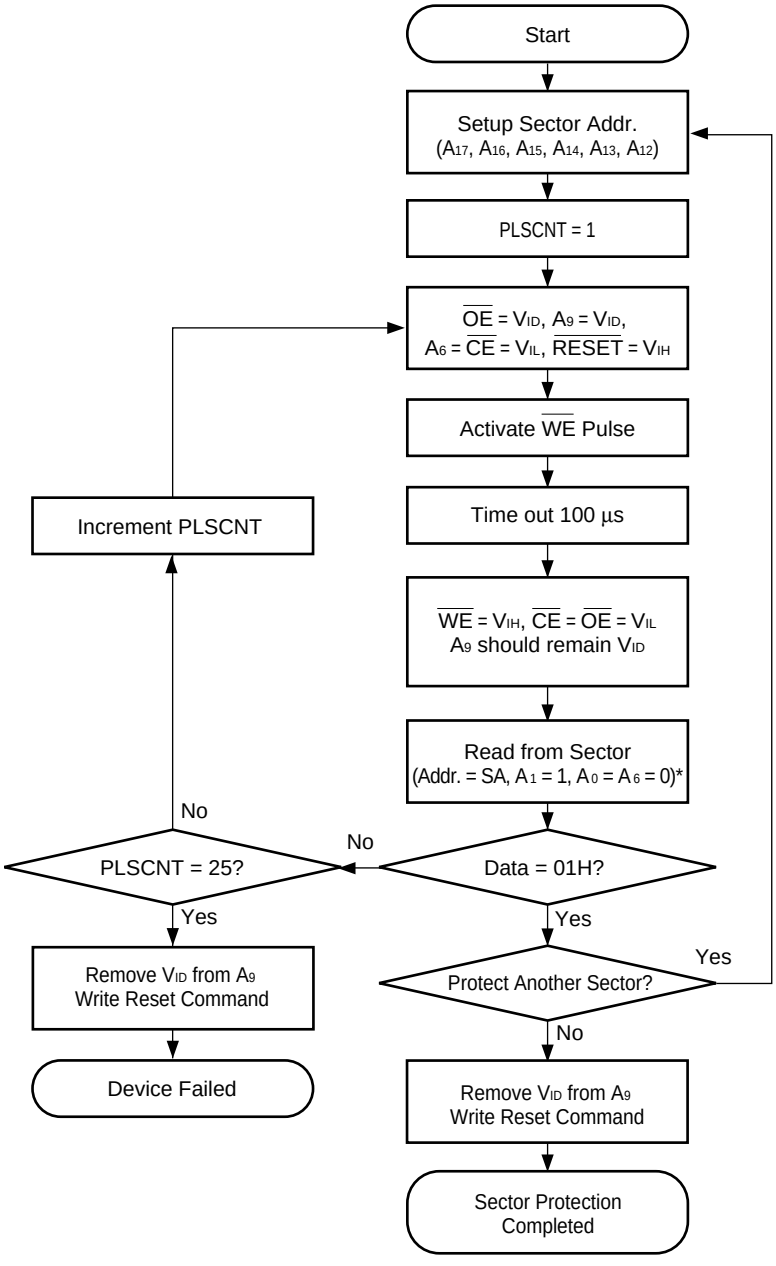
Figure 20 $\overline{\text{Data}}$ Polling Algorithm



VA = Byte address for programming.
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation.
= XXXXH during sector erase or multiple sector erases operation.
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

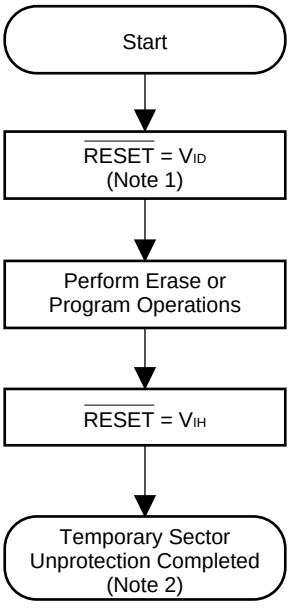
Note: DQ_6 is rechecked even if DQ_5 = “1” because DQ_6 may stop toggling at the same time as DQ_5 changing to “1”.

Figure 21 Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

Figure 22 Sector Protection Algorithm



Notes: 1. All protected sectors are unprotected.
2. All previously protected sectors are protected once again.

Figure 23 Temporary Sector Unprotection Algorithm

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Word Programming Time	—	16	5,200	µs	Excludes system-level overhead
Byte Programming Time	—	8	3,600		
Chip Programming Time	—	4.2	T.B.D	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	Cycles	—

■ TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	9.5	12.5	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	9.5	12.5	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SON PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	T.B.D	T.B.D	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	T.B.D	T.B.D	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	T.B.D	T.B.D	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

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